Contamination Control and Protocol

---- NFF training (Part C)

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How to become an NFF user?

Part A - Safety Training

Part B - Chemical Safety
(Self learning program MC07 and MC03 by HSEO)

Part C - Contamination Control and Protocol

Part D - NFF Web Site and Booking System

NFF Examination

Make an appointment with Ms Terry LAM

Process Flow Proved by NFF

NFF access card

For more information, please visit NFF website: http://www.nff.ust.hk

NFF user

Services

Safety training
NFF Examination

- Time: 150 minutes
- Open Book
- Passing Marks:

<table>
<thead>
<tr>
<th>✓ Qualify questions</th>
<th>2 mc*</th>
<th>100%</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓ Part I Safety (Part A)</td>
<td>25 mc*</td>
<td>60%</td>
</tr>
<tr>
<td>✓ Part II Contamination Control and Protocol</td>
<td>25 mc*</td>
<td>60%</td>
</tr>
<tr>
<td>(*multiple choice—单项选择)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>✓ Part III Process Flow</td>
<td>2 PF</td>
<td>60%</td>
</tr>
</tbody>
</table>

5 mistakes / PF
The syllabus of NFF examination

**Part I Topics:**
- Cleanroom Environment
- MSDS & Material Restriction
- Alarm System and Emergency Escape Route
- General Lab Safety
- Fire and Chemical Safety
- Equipment and Operation Safety

**Part II Topics:**
- Contamination Control
- Process Verification Scheme
- General Process Requirements
- Operation Guidelines
- Cleanliness Levels of Equipment and Wafer Status

**Part III Topics:**
- Paper II Topics
- Standard Format of Process Flows
Outline

1. Introduction to cleanroom & NFF
2. Contamination Control
3. Process modules in NFF
4. Process flow
5. Discussion
Introduction to cleanroom [1]

A clean environment is designed to reduce the contamination of processes and materials. Air flow rates and direction, pressurization, temperature, humidity and specialized filtration all need to be tightly controlled.

Clean-room ventilation: Two flow systems

- Turbulent
- Laminar
cleanroom standard in US

- the US government issued Fed. Std. 209 (now 209E) to standardize cleanroom design in 1963

**English Units (particles/ft³)**

<table>
<thead>
<tr>
<th>Class</th>
<th>0.1μm</th>
<th>0.2μm</th>
<th>0.3μm</th>
<th>0.5μm</th>
<th>5.0μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3.5x10¹</td>
<td>7.5</td>
<td>3.0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>3.5x10²</td>
<td>7.5x10¹</td>
<td>3.0x10¹</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>7.5x10²</td>
<td>3.0x10²</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1,000</td>
<td>1,000</td>
<td>7.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10,000</td>
<td>10,000</td>
<td>7.0x10</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Metric Units (particles/m³)**

<table>
<thead>
<tr>
<th>Class</th>
<th>0.1μm</th>
<th>0.2μm</th>
<th>0.3μm</th>
<th>0.5μm</th>
<th>5.0μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>3.5x10²</td>
<td>7.6x10¹</td>
<td>3.1x10¹</td>
<td>1.0x10¹</td>
<td></td>
</tr>
<tr>
<td>M2</td>
<td>3.5x10³</td>
<td>7.6x10²</td>
<td>3.1x10²</td>
<td>1.0x10²</td>
<td></td>
</tr>
<tr>
<td>M3</td>
<td>3.5x10⁴</td>
<td>7.6x10³</td>
<td>3.1x10³</td>
<td>1.0x10³</td>
<td></td>
</tr>
<tr>
<td>M4</td>
<td>7.6x10⁴</td>
<td>3.1x10⁴</td>
<td>1.0x10⁴</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M5</td>
<td>1.0x10⁵</td>
<td>6.2x10²</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Introduction to NFF [3]

- The first nanofabrication laboratory established at a tertiary institution in Hong Kong since 1991.

- Its mission is to provide fabrication facilities in support of research and teaching in micro/nano devices and systems. NFF aims to support not only individual faculty members of HKUST but also researchers from local institutions in the area of micro/nano devices and systems.

- Mainland and overseas institutions as well as private sectors are also welcome to approach NFF for technical collaborations.
Introduction to NFF [4]

**Phase II**
- Area: 750m²,
- Class 100, class 1000 and class 10,000.
- **5 Equipment modules:**
  - Mask making
  - Photolithography
  - Wet etching and CMP
  - Dry Etching and Sputtering
  - Thermal processing and implantation

**Phase III-EC**
- Phase III (Enterprise Center) area is 200m² opened in 2009.
- **Main equipment modules** (Non-std):
  - E-beam lithography
  - Basic photolithography
  - E-beam evaporation and sputtering
  - Wet etch and lift-off

**Rm.2223/2227**
- Room 2223
- Deep RIE process center
- Room 2227
- TSV Process Laboratory
- Electroplating
- Grinding and Polishing

**Location:**
- P200100, P201000
- EC01000
- Rm.2223/Rm.2227

*Nanosystem Fabrication Facility,*
*The Hong Kong University of Science and Technology*
Process modules in NFF

**Photolithography**
- Laser direct writer
- Stepper
- Contact aligner
- Substrate bonder
- Wafer tracks
- Resist coaters
- E-beam lithography
- Nanoscibe 3D printer
- SEM
- Microscopes
- Wet stations
- Ovens/hot plates

**Wet etching & CMP**
- Wet Stations
  - Cleaning
  - Metal etch
  - Si etch
  - PR strip
  - CMP, oxide and Polysilicon
  - CMP, metal
  - Wafer grinder
  - Wafer polisher
  - Electroplating

**Dry etch & Sputter**
- ICP etchers
  - SiO₂
  - Polysilicon
  - Si DRIE
  - GaN
  - Metals
  - RIE etchers
  - XeF₂ Etcher
  - Metal sputtering
  - E-beam evaporators
  - O₂ ashers

**Thermal & Implant**
- Furnaces
  - Oxidation
  - Diffusion
  - LPCVDs
  - RTPs
  - PECVDs
  - SiO₂
  - Nitride
  - Amor-Si
  - CNT
  - Silicon Epitaxy
  - ALD
  - Ion Implanters
Research areas in NFF

Departments we are serving:

- Electronic & Computer Engineering
- Mechanical and Aerospace Engineering
- Physics
- Chemical and Biological Engineering
- Department of Chemistry
- Division of Life Science
- Nano and Advanced Materials Institute

Main research areas we are supporting:

- Microelectromechanical Systems (MEMS)/Sensors
- III-V electronics (HEMT, LED, Laser)
- Display Technology (OLED, TFT, LCD)
- Bio/life science/ Microfluidics
- CNT, Graphene. 2D material
- MOSFET, bipolar, inductor
- Photonics
- Solar Cell
- Advanced packaging
Contamination Control

- What is contamination?
- How to Minimize Contamination?

  - Proper Cleanroom Protocol
  - Process Verification Scheme
    - Three Cleanliness Levels
      --Clean
      --Semi-Clean
      --Non-Standard
    - Downward compatible

Your awareness and observance!!
What is contamination?

- **Contamination** is the intrusion of impurities into devices that leads to their failure.

- **3 Commonest Contaminants**
  - Particles
  - Metal ions
  - Organics

- **Examples:**
  - Degradation of Oxide Integrity
  - Threshold Voltage Shift
  - Leakage Current
3 Commonest Contaminants

- **Particles**
  - People ~75%
  - Ventilation ~15%
  - Room Structure ~5%
  - Equipment ~5%
  - Metal pieces from lift-off wafers
  - You name it

- **Metallic Contaminants**
  - Ions of heavy and transition metals (Au, Ag, Pt, Ni)
  - Ions of standard Metal (Al, Ti, Mo)
  - Alkali Ions (K, Na)

- **Organics**
  - Photoresist and Polymers
  - Body Oil

Peeling of Polymer

Particle caused defects in metal lines
Knock-on Effect

Contaminants

Bath for Resist Strip

Cleaning Bath

Tools e.g. Cassette

Clean/Semi-Clean

Furnace A

Furnace B

Etcher A

Bath for Resist Strip

Clean/Semi-Clean
Why contamination matters to you?

- It’s like disease, easy to spread across the entire laboratory
- It’s hard to be found and initialized
- It’s hard to be stopped once caused
- Any contamination you cause ruins others’ years of efforts
- You are the only one who can help us stop it from spreading

The success of each user relies on trust, understanding and shared responsibility among all users.
Cleanroom Protocol

Purpose

- Promote successful Cleanroom Operations
- Ensure safety in the Cleanroom Environment
- Provide Operational Conditions that Meet Process & User needs

Perspective

- The protocol provides basic awareness and general guidelines for cleanroom users
- Successful clean room operation relies on each user’s understanding, participation and self discipline
- The success of each user relies on trust, understanding and shared responsibility among all users
Cleanroom Gowning Procedure

**Step 1: Pre-entry**

- **A** Bouffant/Hair Net
  Be sure to contain all hair.

- **B** Shoe Covers
  Contain all laces and tassels.

**Step 2: Gowning**

- **A** Gowning Gloves
  Recommended for Class 100 and better.

- **B** Mask
  Worn over or under hood. Bend nosepiece first for a snug facial fit.

- **C** Hood
  Ensure snug fit and proper face/neck seal.

**Step 3**

- **Coverall**
  Step into the coverall.
  Be sure sleeves and upper garment do not touch bench or floor.
  Tuck shoulder panels from hood inside coverall before zipping up.

**Step 4**

- **Boot Covers**
  Put on boots and pull boots (high-top shoe covers) over legs of coverall.
  If cross-over bench is used, transfer each foot to cleaner side of bench as boot is donned.

**Step 5**

- **Goggles**
  Wear goggles/safety glasses when eye protection or additional particulate control is desired.

**Step 6**

- **Cleanroom Gloves (optional)**
  Place hem of glove over cuff of sleeve. Put on over gowning gloves or remove gowning gloves and then put on cleanroom gloves.

The diagram is from DuPont®
Cleanroom Gowning Removal Procedure

**Step 1:** In Order

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gloves</td>
<td>Goggles/Safety Glasses</td>
<td>Boot Covers</td>
</tr>
<tr>
<td>If two pairs of gloves are worn, remove top pair of gloves, then discard.</td>
<td>Remove and properly contain.</td>
<td>Usually discard after each change.</td>
</tr>
</tbody>
</table>

**Step 2**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coverall</td>
<td>Hood</td>
<td>Mask</td>
</tr>
<tr>
<td>If coverall is to be used again, either hang it in a controlled environment or prepare for storage.</td>
<td>Hang in controlled environment.</td>
<td>Remove and usually discard.</td>
</tr>
</tbody>
</table>

**Step 3**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gloves</td>
<td>Bouffant/Hair Net</td>
<td>Shoe Covers</td>
</tr>
<tr>
<td>It is recommended that gloves be discarded after each change.</td>
<td>Usually discard after each change.</td>
<td>Usually discard after each change.</td>
</tr>
</tbody>
</table>

The diagram is from DuPont®
## Activity and Particle Generation

### Relationship of activity to the number of particles shed from a human body

<table>
<thead>
<tr>
<th>Activity</th>
<th>Number of particles generated (0.5µm and larger per min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sitting or standing still</td>
<td>100 000</td>
</tr>
<tr>
<td>Sitting, small movement of arms or head</td>
<td>500 000</td>
</tr>
<tr>
<td>Sitting, moving arms, legs or head</td>
<td>1 000 000</td>
</tr>
<tr>
<td>Standing up</td>
<td>2 500 000</td>
</tr>
<tr>
<td>Walking slowly</td>
<td>5 000 000</td>
</tr>
<tr>
<td>Walking normally</td>
<td>7 500 000</td>
</tr>
<tr>
<td>Walking with speed (2.5m/s)</td>
<td>10 000 000</td>
</tr>
<tr>
<td>Performing work-out</td>
<td>15 000 000-30 000 000</td>
</tr>
</tbody>
</table>

### Number of particles found in cosmetics

<table>
<thead>
<tr>
<th>Type of cosmetics</th>
<th>Number of particles per application (Particle size 0.5µm and larger)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lipstick</td>
<td>1 100 000 000</td>
</tr>
<tr>
<td>Rouge</td>
<td>600 000 000</td>
</tr>
<tr>
<td>Powder</td>
<td>270 000 000</td>
</tr>
<tr>
<td>Eye shadow</td>
<td>82 000 000</td>
</tr>
<tr>
<td>Mascara</td>
<td>3 000 000 000</td>
</tr>
<tr>
<td>In total for one application</td>
<td>5 100 000 000</td>
</tr>
</tbody>
</table>

Process Verification Scheme—Cleanliness levels

- Every thing in NFF
  - Chemicals
  - Materials
  - Wafers/Substrates
  - Equipment and Machines

- Three cleanliness levels classified according to their contamination risks
  -- Clean
  -- Semi-Clean
  -- Non-Standard

- 6 equipment Combinations
Contamination Risks & 3 Cleanliness Levels

**Low Risk**

No contaminants. Silicon wafer & SOI wafer (bought from NFF), SiO₂, SiNx, Ge, etc.

**Semi-Clean**

<table>
<thead>
<tr>
<th>Material</th>
<th>Material</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>Mo</td>
<td>Ti</td>
</tr>
<tr>
<td>Cr</td>
<td>Ni for MILC</td>
<td></td>
</tr>
<tr>
<td>ITO</td>
<td>ZnO</td>
<td>IGZO</td>
</tr>
<tr>
<td>MILC wafers</td>
<td>High-quality glass (Corning 1737 or better)</td>
<td></td>
</tr>
</tbody>
</table>

**Non-Standard**

<table>
<thead>
<tr>
<th>Material</th>
<th>Material</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>MoS</td>
<td>Cu</td>
<td>GaAs/Ga Nitirde,</td>
</tr>
<tr>
<td>Fe</td>
<td>Au</td>
<td>Pt</td>
</tr>
<tr>
<td>Ag</td>
<td>KI</td>
<td>KOH, Na⁺</td>
</tr>
<tr>
<td>Low quality glass</td>
<td>PCB boards, (photo only)</td>
<td></td>
</tr>
<tr>
<td>Wafers undergone any processes at/with Non-Standard Equipment</td>
<td>Non-NFF-standard chemicals, such as, Polyimide, SU-8, BCB, PDMS, and so on</td>
<td>Wafers undergone lift-off</td>
</tr>
<tr>
<td>Materials or chemicals not yet classified.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Process Verification Scheme

- Cleanliness of wafer is regarding to process history and changes as the fabrication process.

- Downward Compatible with equipment
  - Clean -> Clean or Semi-Clean or Non-Standard
  - Semi-Clean -> Semi-Clean or Non-Standard
  - Non-Standard -> Non-Standard

- But not the Reverse !!!

  ❌ Non-Standard -> Semi-Clean -> Clean
    - Once contaminated always contaminated
Downward Compatible Mechanism

Clean

- Clean
  - Clean / Semi-Clean
  - Clean / Semi-Clean / Non-Standard
  - Semi-Clean
  - Semi-Clean / Non-Standard
  - Non-Standard

Semi-Clean

- Clean / Semi-Clean
  - Clean / Semi-Clean / Non-Standard
  - Semi-Clean
  - Semi-Clean / Non-Standard
  - Non-Standard

Non-Std

- Clean / Semi-Clean
  - Clean / Semi-Clean / Non-Standard
  - Semi-Clean
  - Semi-Clean / Non-Standard
  - Non-Standard

Nanosystem Fabrication Facility,
The Hong Kong University of Science and Technology
One exception--Decontamination

- Wafers for decontamination
  - Post Chemical-Mechanical Planarization (CMP) wafers
- How to do decontamination?
  - Wet station B3 (RCA1): NH₄OH:H₂O₂:H₂O (1:1:5) 70 °C
- Wafer Status after decontamination
  - Clean
- Not Suitable for:
  - Non-standard Wafers
  - Almost all Semi-Clean Wafers
Gold Ions

- Most-Contaminating because of its high mobility
- Easy to spread into the atmosphere, if heated
- From films, equipment, tools, containers and cassettes, which are in contact with Au+ ions
- Make it as close to the last step as possible.
- Never put gold-contaminated samples into Clean and Semi-Clean areas, (in particular sulfuric acid for resist stripping). Otherwise you will kill the whole laboratory!
Contamination arising from Integration

- **Inter-level Contamination**
  - Caused by contaminants from incompatible cleanliness groups
  - E.g. Non-standard group contaminates Semi-clean group

- **Intra-level Contamination**
  - Caused by contaminants from the same cleanliness level
  - Heavily Doped Photoresist/PSG Vs some CLEAN equipment
  - Cr/Al/ITO vs Some SEMI-CLEAN equipment
  - PCB boards vs Non-Standard Sputters

- **Extra-level Contamination**
  - Caused by contamination sources other than the above
  - E.g. Photoresist, Particles, Body Oils, to name but a few
How to deal with a new material or new process?

- Two-level “Contamination Control Review Panel”

- NFF internal review panel
  - Members: (NFF staff) Wing Leong CHUNG, Preason M W LEE, Shuyun ZHAO, and a Senior Technician in charge of the equipment
  - Aim: To evaluate the new material risks to a particular equipment

- Faculty review panel
  - Members: Prof. Kei May LAU (ECE), Prof. Jiannong WANG (PHYS), Prof. Ho Bun CHAN (PHYS)
  - Aim: To evaluate the new material risks to NFF lab

- Evaluated by NFF internal review panel
- Evaluated by faculty review panel
- NFF PIs/Users Consultation
- Make final decision by NFF internal review panel
Process modules in NFF

1. Photolithography
2. Cleaning and Wet etching
3. Thin film growth and Deposition
4. Implantation
5. Dry Etching
6. Grinding and Polishing
7. Metrology
Fabrication process

Realize your designed device!!

Ready for next layer of deposition

Repeat above processes

(Courtesy of IBM Research.)
Photolithography [1]

**Step 1: Photoresist coating**
1. Spin coating
2. Spray coating

**Step 2: Exposure**
1. Contact Aligner (1:1)
2. Stepper (5:1)

**Step 3: Develop**
1. SVG Developer Track
2. Manual develop

**Step 4: Etch**
1. Wet etch
2. Dry etch

**Step 5: PR strip**
1. Sulfuric acid
2. MS2001
3. O₂ plasma

Positive Resist

Negative Resist/Dual-tone Resist
From design to photo mask

1. Design structure and layout using computer

2. Stream out single layer layout
Submit job request though website

3. Make photomask using Laser direct writer

4. To start...
Mask Making

- Pattern generation using a CAD program (Cadence, L-edit, Silvaco, etc.), to get a layout file (.gds/.cif format)
- Submit your job request through NFF website
- Written by laser direct writer ($HKD750/mask)
- Different masks can be generated using the same layout

https://nanolab.ust.hk/booking/navmain.asp

Nanosystem Fabrication Facility, The Hong Kong University of Science and Technology
1. Two small squares located at (0,0) and (10000, 10000) to define the original position
2. Design your own align mark and testing structures
3. Mirror your layout before submission
4. Check your new mask carefully before you use it
Contact Aligner

Karl Suss MA6 #1, #2

AB-M Aligner #1, #2
Mask for ASML Stepper

Patterns you designed

× 5 and mirror the pattern

Stepper Mask

Mask in equipment

Patterns on wafer

Exposure using ASML stepper
<table>
<thead>
<tr>
<th><strong>Light source illumination</strong></th>
<th>i-line (365 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Resolution</strong></td>
<td>0.5 µm</td>
</tr>
<tr>
<td><strong>Maximum writing error</strong></td>
<td>± 0.1 µm (3σ)</td>
</tr>
<tr>
<td><strong>Wafer size</strong></td>
<td>4&quot; or 6&quot;</td>
</tr>
<tr>
<td><strong>Field size</strong></td>
<td>15 mm x 15 mm or 10 mm x 10 mm (on wafer)</td>
</tr>
<tr>
<td><strong>Reduction ratio</strong></td>
<td>5:1</td>
</tr>
<tr>
<td><strong>Photomask size</strong></td>
<td>5&quot; square</td>
</tr>
</tbody>
</table>
Photoresist Coating

Spin-coating

a) Dispensation
b) Acceleration
c) Flow dominated
d) Evaporation dominated

Spray-coating (EVG Spray Coater)

1) An ultrasonic spray nozzle for photoresist dispense
2) An independent rotation chuck.

Improper coverage due to centrifugal spin
Uniform coating with ultrasonic nozzle
SVG Coater Track & Developer Track

- HMDS Prime
- PR coating
- Soft bake
- Coater track
- Develop
- Hard bake
- Developer track
- Cassette for PR coating
SVG Coater Track & Developer Track

**HMDS prime**
- To enhance the adhesion between PR and substrate

**PR spin coating**
- To get uniform photoresist on a substrate, back side and rim cleaning

**Soft bake**
- Partially remove the solvent in PR

**Alignment and Exposure**

**Develop**
- Dissolve the exposed PR/unexposed PR to form pattern

**Hard bake**
- Harden the photoresist for next step
Alignment and Exposure

- **contact printing**

  UV light
  mask
  direct contact
  photoresist

  - simple, but easy to cause mask damage
  - Example: Karl Suss MA6#1, #2, AB-M Aligner #1, #2

- **proximity printing**

  light
  mask
  gap between mask & resist
  photoresist

  - increase mask lifetime, reduce particle, but poor resolution
  - Example: Karl Suss MA6#1, #2

- **projection printing**

  light
  mask
  focusing lens
  photoresist

  ASML Stepper
  - with 5X reduction
  - Minimum line width: 0.3-0.5µm
  - High resolution
  - Long mask lifetime
  - No contact contamination
  - Small exposure area
  - High alignment accuracy
E-beam direct writing

50nm line patterns with 0.3° rotation angle

JEOL JBX-6300FS E-Beam Lithography System

More detailed information, please contact with Mr. Nelson LI
Email: eenelson@ust.hk
Develop

1. **SVG Developer track**
   - Chemical: FHD-5
   - Time=60s
   - Suitable for Most of positive photoresist

2. **Wet Z1:FHD-5**
   - Chemical: FHD-5
   - For Semi-Clean wafers which can not be developed on SVG track

3. **Wet W2/M (EC01000):**
   - Chemical: FHD-5
   - For Non-Standard wafers

4. **Other Developer: AZ 400K** (only for PR AZ 4903)
   - Can be operated on the Wetsation W, Z, X and M
# Soft & Hard Bake (hot plate & oven)

**Hot plate**

<table>
<thead>
<tr>
<th>Hot Plate Bake</th>
<th>Oven Bake</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single wafer</td>
<td>Batch</td>
</tr>
<tr>
<td>Short time/wafer</td>
<td>Long time/batch</td>
</tr>
<tr>
<td>No photoresist on backside</td>
<td>No requirements</td>
</tr>
</tbody>
</table>

**Oven**

- **Cassette for oven**
Resist Strip

1. Sulfuric Acid (120 °C H₂SO₄ + H₂O₂ 10min)

   Wet E4: Clean /Semi-clean, No metal or silicides
   **Process:** Sulfuric Acid 10min ->Dump-rinse ->Spin Dry
       ->Inspection
   **Safety:** Sulfuric Acid (H₂SO₄)): Corrosive
   Hydrogen peroxide (H₂O₂: strong oxidizer)

2. MS2001: 70° C 5min (after metallization)

   Wet Y1: Semi-Clean
   Wet W1/M1: Non-Standard
   **Process:** Sulfuric Acid 10min ->Dump-rinse ->Spin Dry
       ->Inspection
3. O₂ Plasma Asher: (After Dry etch, ion implantation)

PS210 Asher: Clean
IPC 3000 Asher #1: Semi-Clean
IPC 3000 Asher #2: Non-Standard

Process:
Dry: O₂ plasma asher ~25min

\[ C_nH_yO_z + O \rightarrow CO + CO_2 + H_2O \]

Wet: Sulfuric Acid 10min / MS2001 5min
Dump-rinse
Dry with N₂
Inspection
Lift-off process

1. Normally used for research
2. Not a standard industry process
3. Suitable for films which are difficult to be etched
4. Low yield due to the film pieces re-deposition
5. Retrograde resist edge profile or large resist/film thickness ratio is needed
6. Multiple layer resist can also be used to generate the undercut (LOL 2000+PR)
7. Film thickness is limited by the resist thickness
8. Film deposition method is limited by the process (e-beam evaporation or limited sputter system)
Guideline for lift-off process

- Pattern size of lift-off process: >1µm
- Lift-off resist: Dual-tone photoresist
  - AZ5206, thickness: 0.8~1.2µm;
  - AZ5214, thickness: 1~3µm
- Acetone, and IPA used should be poured into dedicated waste bottles in Wetstation Z
- Make it the last step
- Once lift-off is done, the samples can’t stop generating contaminants
Safety issues about photolithography

- Contamination caused by photoresist
- Inhalation of Organic Vapors and Solvent
  a) HMDS—Flammable and explosive
  b) FHD-5—Poisonous and corrosive,
  c) UV light—Can cause eye injury if direct look at UV source
- No acid nor base in Yellow Room
- Coater and developer Tracks not for double-side photoresist coating, and negative photoresist
- Disposal of Waste (IPA, Acetone)
  ▪ Pour the waste into waste collection bottles
  ▪ Don’t use an aspirator to suck it into the N-tank
- Containers used for developing or any process require booking on the computer system.
- Transparency only allow on AB-M 2
Process modules in NFF

1. Photolithography
2. Cleaning and Wet etching
3. Thin film growth and deposition
4. Implantation
5. Dry Etching
6. Grinding and Polishing
7. Metrology
Layout of Wet Stations in Phase II

**Cleanliness levels**
- Clean
- Semi-Clean
- Non-Standard

**Wetstation J**
- J1
- J2

**Wetstation G**
- G1
- G2

**SRD-G**
- Water Rinsing

**Wetstation Y**
- Y1
- Y2

**SRD-Y**
- Water Rinsing

**Wetstation X**
- X1
- X2

**SRD-X**
- Water Rinsing

**Wetstation W**
- W1
- W2

**SRD-W**
- Water Rinsing

**Wetstation Z**
- Z1
- Z2

**SRD-Z**
- Water Rinsing

---

**A – Sulfuric Cleaning Station**
- A1: Sulfuric Cleaning (NFF reserved)
- A2: HF:H₂O (1:50) (For diffusion)
- A3: Sulfuric Cleaning (Only for “Clean” furnace & RTP)

**B – Sulfuric Cleaning/Decontamination Station**
- B1: Sulfuric Cleaning (Not for “Clean” furnace & RTP)
- B2: HF:H₂O (1:50)
- B3: Decontamination

**C – Oxide/Nitride Etching Station**
- C1: Nitride Strip
- C2: Oxide Deglaze/PSG Removal
- C3: BOE

**D – Semi-Clean Metal Processing Station**
- D1: Aluminum Etch
- D2: HF:H₂O (1:100) MILC
- D3: General Purpose
- D4: Sulfuric Cleaning for MILC

**E – Semi-Clean Non-Metal Processing Station**
- E1: ITO Etch
- E2: General Purpose
- E3: HF:H₂O (1:100)
- E4: Resist Strip

---

**F – Non-Standard Processing Station**
- F1: General Purpose
- F2: General Purpose
- F3: General Purpose

**G – TMAH Etching Station**
- G1: TMAH (up to 80°C)
- G2: TMAH (up to 80°C)

**J – Non-Standard processing station**
- J1: TMAH/KOH Etching
- J2: TMAH/KOH Etching

**X – Clean Organic Solvent Station**
- X1: General Purpose
- X2: General Purpose

**Y – Semi-Clean Organic Solvent Station**
- Y1: MS2001 Resist Strip
- Y2: MS2001 Mask Cleaning

**Z – Semi-Clean/Non-Standard Organic Solvent Station**
- Z1: FHD-5 (Semi-Clean)
- Z2: Dump Rinser (Semi-Clean/Non-Standard)

**W – Non-standard Organic Solvent Station**
- W1: MS2001 Resist strip
- W2: FHD-5 Developing
Wet stations

Chemical Tank

DI water for rinsing

Spin Rinser Dryer (SRD)

Cabinet for container and cassette
Labels of Wet Stations

A: Sulfuric Cleaning Station
B: Sulfuric Cleaning/Decontamination Station
C: Oxide/Nitride Etching Station
G: TMAH Etching Station
X: Clean Organic Solvent Station
E: Semi-Clean Non-Metal Processing Station
D: Semi-Clean Metal Processing Station
Y: Semi-Clean Organic Solvent Station
Z1: Semi-Clean Develop Station
Z2: Semi-Clean/Non-standard Dump Rinser
F: Non-Standard Processing Station
J: Non-Standard Processing Station
W: Non-Standard Organic Solvent Station

Lowest Risks of Contamination

Nanosystem Fabrication Facility,
The Hong Kong University of Science and Technology
Cleanings of Sample

Clean

- Sulfuric Cleaning for “Clean” furnace and RTP (A3)
- HF dip before oxide growth (A2)
- Normal Sulfuric Cleaning (B1)
- HF dip (B3)
- RCA1 (Decontamination) (B3)

Semi-Clean

- Sulfuric Cleaning (D4) (Semi-Clean)
- Post-Metallization Cleaning—(MS2001) (Y1)
- Mask Cleaning (MS2001) (Y2)

Non-Standard

- Normal cleaning (MS2001 or DI water) (W2, F, M)
Sulfuric Cleaning / Piranha etch

- (Piranha solution) $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$, $120^\circ\text{C}$ 10min
- Removing organics and gross contaminants e.g. scribe dust.
  - $\text{H}_2\text{SO}_4$ – reduces organics to carbon
  - $\text{H}_2\text{O}_2$ – oxidizes carbon to form $\text{CO}_2$

- Very dangerous, being both strongly acidic and a strong oxidizer.
- Both liquid and vapor are extremely corrosive to skin and respiratory tract.
- When preparing the Piranha solution, always add the peroxide to the acid.
HF dip

Process:
- HF:H₂O (1:50) Time: 1min
- Room Temperature
- 4-cycle Dump rinse
- Spin Dry

To remove the native or chemical oxide on the silicon surface.

Prior to the growth of high quality oxide
Clean Cleaning Station A&B

- **Wetsation A**: Only for the cleaning prior “Clean” furnace and RTP process
  - Wafer has to be “Clean”
  - No photoresist
  - All wafers have to be dried using Spin Dryer-A.
  - After cleaning, wafers can ONLY be sent to “Clean” furnace and RTP

- **Wetsation B**: For other purpose except “Clean” furnace and RTP process
  - Wafer has to be “Clean”
  - No photoresist
  - All wafers have to be dried using Spin Dryer-B.
  - After cleaning, wafers CANNOT be sent to “Clean” furnace and RTP
RCA1 (Decontamination)

- “Clean” or Decontaminatable Wafers (Post CMP wafers)
- No photoresist, metals
- **Wet B3**: Decontamination
  - $\text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{NH}_4\text{OH} = 5:1:1$ at $70 \degree \text{C}$ (fresh)
- Drain after use
- To removes organics, particles
Post-Metal Cleaning

- **MS2001, 70°C, 5min**

- **Process:**
  - Clean wafers with MS2001 in Bath Y1 (for Semi-Clean) or W2 (Non-Standard) (Optional)
  - 4-cycle DI water dump rinser
  - Spin wafers Dry with Spin Rinser Dryer or Dry using N₂ gun

⚠️ Don’t use sulfuric cleaning after metallization!!
Mask Cleaning

- Semi-Clean
- Mask Only

Process:
- **Wet Y2**:MS2001,
- @70°C, 5min
- Dump-rinse 4 cycles
- Dry by an N₂ Gun
- Oven bake (105°C, 10min)
- Cool down to room temperature

Oven for mask bake
Cleaning policy prior to high temperature process

- Wet Cleaning is required (For Furnace, PECVD, RTP)
- Cleans must be done less that 1 hour before equipment loading and wafers must be stored in clean Teflon cassettes in white box
- Wafers can move between equipment of equal cleanliness (or to lower cleanliness level) – if interval is less than 1 hour – wafers are in a clean Teflon cassette in white box (not plastic)
# Typical Wet Etchants in NFF

<table>
<thead>
<tr>
<th>Material</th>
<th>Chemical</th>
<th>Etching Rate</th>
<th>Mask</th>
<th>Selectivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al/Si-1%</td>
<td>$\text{H}_3\text{PO}_4:\text{CH}_3\text{COOH:HNO}_3=100:10:1 \ (50^\circ\text{C})$</td>
<td>2823A/min</td>
<td>PR</td>
<td>&gt;50</td>
</tr>
<tr>
<td>Ti-W</td>
<td>$\text{H}_2\text{O}_2\ (60^\circ\text{C})$</td>
<td>1000A/min</td>
<td>SiO2</td>
<td>&gt;50</td>
</tr>
<tr>
<td>Ti</td>
<td>$\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HF} \ (20:1:0.5)$ $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} \ (1:1:5)$</td>
<td>5400A/min 231A/min</td>
<td>PR</td>
<td>&gt;50</td>
</tr>
<tr>
<td>Cr</td>
<td>MTI CEP-200 chrome etchant</td>
<td>1320/min</td>
<td>PR</td>
<td>&gt;50</td>
</tr>
<tr>
<td>Si3N4</td>
<td>Hot $\text{H}_3\text{PO}_4 \ (165^\circ\text{C})$</td>
<td>41.3A/min</td>
<td>&gt;50</td>
<td></td>
</tr>
<tr>
<td>Wet SiO2</td>
<td>BOE 777 Pad etch $\text{HF:H}_2\text{O}=1:100$</td>
<td>1000A/min 330A/min 27A/min</td>
<td>PR</td>
<td>&gt;50</td>
</tr>
<tr>
<td>LTO</td>
<td>BOE 777 Pad etch $\text{HF:H}_2\text{O}=1:100$</td>
<td>3000~5000A/min 1500A/min 100A/min</td>
<td>PR</td>
<td>&gt;50</td>
</tr>
<tr>
<td>Poly-Si</td>
<td>Freckle</td>
<td>200A/min</td>
<td>PR</td>
<td>&gt;50</td>
</tr>
<tr>
<td>a-Si</td>
<td>Freckle</td>
<td>200A/min</td>
<td>PR</td>
<td>&gt;50</td>
</tr>
<tr>
<td>C-Si (100)</td>
<td>25% TMAH (80°C)</td>
<td>20µm/hr</td>
<td>Nitride/oxide</td>
<td>&gt;50</td>
</tr>
<tr>
<td>ITO</td>
<td>HCL+$\text{H}_2\text{O}+\text{HNO}_3=4:2:1$</td>
<td>80A/min</td>
<td>PR</td>
<td>&gt;50</td>
</tr>
</tbody>
</table>

[http://www.nff.ust.hk/equipment-and-process/process/WetDryEtchingTable.htm](http://www.nff.ust.hk/equipment-and-process/process/WetDryEtchingTable.htm)
Etching Through Wafers

- **TMAH**
  - “Clean” Process
  - Nitride + Oxide as Etching Masks

- **KOH**
  - Etching furiously
  - Non-Standard Process

- **Dry Etch**
  - Deep RIE Etcher
  - Clean Process

A square-shaped cavity on (100)-Si Wafer after TMAH etching
Wet Stations

- **General Safety**
  - No chemicals bottle left on the floor
  - Wafers have to be dump-rinsed in the dump-rinser for at least 4 cycles immediately after any chemical processes
  - No organic solvent (IPA, Acetone) in Class 1000 area

- **HF**
  - Highly hazardous Chemical Solutions (HF, BOE, 777 and Freckle etch)
  - Concentration below 20% is more insidious and symptoms may be delayed for up to 24 hours (Refer to Health and Safety Manual—3 Special Guideline on HF Safety)

- **Use of Chemical**
  - Unconventional use of chemical requires **permission** and **booking**.
  - Mixing own chemicals is only allowed at semi-clean or non-standard wetstation

- **Disposal**
  - HF, Freckle Etch and BOE are needed to be drained into the HF tank by NFF staff.
  - Acid and Base are needed to be drained by users themselves with an aspirator in wetstations.

- **Contamination**
  - No Glass, Metals and Manual coated wafers at “Clean” wetstations
  - No Metals at the sulfuric acid bath for resist stripping
  - Separation of cassettes, tools containers and gloves from those of different stations
  - No lifted-off wafers put in baths
  - No mess left at wetstations
Chemical Disposal

Actone, IPA → Collection bottle

HF, BOE, Freckle
By NFF staff only

Aspirator 1 → HF tank

Base, Acid
By user

Aspirator 2 → N tank
Process modules in NFF

1. Photolithography
2. Cleaning and Wet etching
3. Thin film growth and deposition
4. Implantation
5. Dry Etching
6. Grinding and Polishing
7. Metrology
Thermal Oxidation

Method to form silicon dioxide
- thermally grown from silicon (good quality)
- deposit by LPCVD/PECVD (poorer quality)

Thermal oxidation of silicon

- **Dry oxidation:**
  \[ \text{Si}(\text{solid}) + \text{O}_2(\text{gas}) \rightarrow \text{SiO}_2(\text{solid}) \]

- **Wet oxidation:**
  \[ \text{Si}(\text{solid}) + 2\text{H}_2\text{O}(\text{gas}) \rightarrow \text{SiO}_2(\text{solid}) + 2\text{H}_2(\text{gas}) \]
  
  **Temperature:** 800°C-1100°C
  **Thickness:** <3μm.

  Thin oxide (<50nm): Dry oxidation
  Thick oxide (>50nm): Dry-wet-dry sequence.

Silicon consumed during oxidation:
\[ X_{Si} \approx 0.45X_{ox} \]

- Wet oxidation is faster because water molecules are smaller than \( \text{O}_2 \) and easier to diffuse to the Si surface
- Fast process tends to give more surface roughness

![Diagram showing the thermal oxidation process with oxide formation on silicon substrate.](image-url)
Selective oxidation

- also known as LOCal Oxidation of S ilicon (LOCOS)

- nitride can be use as a mask to prevent oxygen/water diffusion in certain region of the wafer to achieve selective oxidation
- nitride and silicon has very different crystal structure and thermal coefficient and should be avoid to be put in direct contact (hence a buffer oxide is usually placed in between)
- should avoid using thick (>200nm) nitride
Diffusion and Annealing

Dopant Diffusion in Silicon

• a general diffusion process

\[ \text{Flux} = D \frac{\partial n}{\partial x} \]

Solid Source

• place a solid source near the wafer in a furnace at an elevated temperature (600°C-1100°C)

Source of Boron C3

\[ 2B_2O_3 + 3Si_2 \rightarrow 4B + 3SiO_2 \]

Source of Phosphorus C2

\[ 2P_2O_5 + 5Si_2 \rightarrow 4P + 5SiO_2 \]
### Thermal oxidation, diffusion and RTP

<table>
<thead>
<tr>
<th>Process Code</th>
<th>Location</th>
<th>Equipment</th>
<th>Cleanliness level</th>
<th>Cleaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DIF-C1</strong></td>
<td>P2-01000</td>
<td>Diff. Furnace-C1 FGA Annealing</td>
<td>Non-Standard</td>
<td>B1+SRD-B/D1(dump-rinser)/F(dump-rinser)</td>
</tr>
<tr>
<td><strong>DIF-C2</strong></td>
<td>P2-01000</td>
<td>Diff. Furnace-C2 N Pre-Deposition</td>
<td>Clean</td>
<td>A3+SRD-A</td>
</tr>
<tr>
<td><strong>DIF-C3</strong></td>
<td>P2-01000</td>
<td>Diff. Furnace-C3 P Pre-Deposition</td>
<td>Clean</td>
<td>A3+SRD-A</td>
</tr>
<tr>
<td><strong>DIF-D1</strong></td>
<td>P2-01000</td>
<td>Diff. Furnace-D1 Dry Oxidation</td>
<td>Clean (Only for gate oxide)</td>
<td>A3+SRD-A</td>
</tr>
<tr>
<td><strong>DIF-A1</strong></td>
<td>P2-01000</td>
<td>Diff. Furnace-A1 Anneal/Oxidation</td>
<td>Clean</td>
<td>A3+SRD-A</td>
</tr>
<tr>
<td><strong>DIF-D2</strong></td>
<td>P2-01000</td>
<td>Diff. Furnace-D2 Dry/Wet Oxidation</td>
<td>Clean</td>
<td>A3+SRD-A</td>
</tr>
<tr>
<td><strong>DIF-D3</strong></td>
<td>P2-01000</td>
<td>Diff. Furnace-D3 Annealing/Dry/Wet Oxidation</td>
<td>Non-Standard</td>
<td>B1+SRD-B/D1(dump-rinser)/F(dump-rinser)</td>
</tr>
<tr>
<td><strong>DIF-D4</strong></td>
<td>P2-01000</td>
<td>Diff. Furnace-D4 Annealing</td>
<td>GaN only</td>
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<tr>
<td><strong>DIF-R1</strong></td>
<td>P2-01000</td>
<td>RTP-600S</td>
<td>Clean</td>
<td>A3+SRD- A</td>
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<tr>
<td><strong>DIF-F1</strong></td>
<td>P2-01000</td>
<td>Diff. Furnace-F1 Annealing/Dry/Wet Oxidation</td>
<td>Semi-Clean</td>
<td>B1+SRD-B D1(dump-rinser)</td>
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<tr>
<td><strong>DIF-C4</strong></td>
<td>P2-01000</td>
<td>Diff. Furnace-C4 FGA Annealing</td>
<td>Semi-Clean</td>
<td>B1+SRD-B D1(dump-rinser)</td>
</tr>
<tr>
<td><strong>DIF-R2</strong></td>
<td>P2-01000</td>
<td>AG610 RTP</td>
<td>Semi-Clean</td>
<td>B1+SRD-B D1(dump-rinser)</td>
</tr>
</tbody>
</table>
Low pressure CVD (LPCVD)

- Low pressure chemical vapor deposition

**Advantages:**
- better purity
- better uniformity
- conformal step coverage

**Applications:**
high temperature oxide, nitride, poly, a-Si, LTO, PSG

**Disadvantage:**
- low deposition rate
- require high processing temperature to increase reaction rate
Plasma Enhanced CVD (PECVD)

- Use RF to discharge the gas and increase reaction rate
- High temperature in LPCVD prevent the use of CVD to deposit material on low temperature substrate (e.g. glass in LCD display) or material (e.g. multi-layer metal)

Advantage: - low temperature
- fast deposition
- good step coverage

Disadvantages: - chemical & particle contamination
- expensive equipment

(STPS 310PC PECVD2)
Atomic Layer Deposition (ALD)

- A method of applying thin films to various substrates with atomic scale precision.
- ALD film growth is **self-limited and based on surface reactions**, which makes achieving atomic scale deposition control possible.

![ALD process diagram](Image)

**Al₂O₃ deposited on silicon trench structures** [1]

# CVD equipment in NFF

<table>
<thead>
<tr>
<th>Process Code</th>
<th>Location</th>
<th>Equipment</th>
<th>Cleanliness level</th>
<th>Cleaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVD-A2</td>
<td>P2-01000</td>
<td>LPCVD-A2 Doped Amor-Si</td>
<td>Clean</td>
<td>A3+SRD-A</td>
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<td>CVD-A3</td>
<td>P2-01000</td>
<td>LPCVD-A3 Amor-Si/Poly</td>
<td>Clean</td>
<td>A3+SRD-A</td>
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<tr>
<td>CVD-B2</td>
<td>P2-01000</td>
<td>LPCVD-B2 Nitride/Low-Stress Nitride</td>
<td>Clean</td>
<td>A3+SRD-A</td>
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<tr>
<td>CVD-B3</td>
<td>P2-01000</td>
<td>LPCVD-B3 LTO</td>
<td>Clean</td>
<td>A3+SRD-A</td>
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<tr>
<td>CVD-EPI</td>
<td>P2-01000</td>
<td>ET3000 Epitaxy</td>
<td>Clean</td>
<td>A3+SRD-A</td>
</tr>
<tr>
<td>CVD-A4</td>
<td>P2-01000</td>
<td>LPCVD-A4 Si-Ge / Amor-Si / Poly</td>
<td>Semi-Clean</td>
<td>B1+SRD-B/D1(dump-rinser)</td>
</tr>
<tr>
<td>CVD-B4</td>
<td>P2-01000</td>
<td>LPCVD-B4 LTO / PSG</td>
<td>Semi-Clean</td>
<td>B1+SRD-B/D1(dump-rinser)</td>
</tr>
<tr>
<td>CVD-F2</td>
<td>P2-01000</td>
<td>LPCVD- F2 Nitride / Low-Stress Nitride</td>
<td>GaN only</td>
<td>B1+SRD-B/D1(dump-rinser)</td>
</tr>
<tr>
<td>CVD-F3</td>
<td>P2-01000</td>
<td>LPCVD- F3 Amor-Si / Poly</td>
<td>Semi-Clean</td>
<td>B1+SRD-B/D1(dump-rinser)</td>
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<tr>
<td>CVD-F4</td>
<td>P2-01000</td>
<td>LPCVD-F4 LTO / PSG</td>
<td>Semi-Clean</td>
<td>B1+SRD-B/D1(dump-rinser)</td>
</tr>
<tr>
<td>CVD-P1</td>
<td>P2-01000</td>
<td>310PC PECVD</td>
<td>Semi-Clean</td>
<td>B1+SRD-B/D1(dump-rinser)</td>
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<td>CVD-TEOS</td>
<td>P2-01000</td>
<td>TEOS PECVD</td>
<td>Semi-Clean</td>
<td>B1+SRD-B/D1(dump-rinser)</td>
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<tr>
<td>CVD-P2</td>
<td>P2-01000</td>
<td>STS PECVD</td>
<td>Non-Standard</td>
<td>B1+SRD-B/D1(dump-rinser)/F(dump-rinser)</td>
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<tr>
<td>CVD-CNT</td>
<td>P2-01000</td>
<td>CNT PECVD</td>
<td>Non-Standard</td>
<td>B1+SRD-B/D1(dump-rinser)/F(dump-rinser)</td>
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<tr>
<td>CVD-ALD</td>
<td>P2-01000</td>
<td>Oxford ALD</td>
<td>Non-Standard</td>
<td>B1+SRD-B/D1(dump-rinser)/F(dump-rinser)</td>
</tr>
</tbody>
</table>
Atoms or molecules of the target material are sputtered off and deposited on a substrate surface. Inert gas such as Ar ions are often used.

DC Sputtering: Metals
RF Sputtering: Insulator, semi-conductor
Magnetron Sputtering: High deposition rate
Reactive Sputtering: SiN_x, SiO_x, ITO

- Relatively good thickness uniformity and step coverage
- Easy thickness control
- Less frequent target change
- Only low-medium vacuum, easy to get impurity
- Limited Target Materials for each Equipment
- Thickness < 3µm
- No photoresist nor broken wafers in Varian 3180 Sputter
- No photoresist in CVC-601 Sputter
**E-Beam Evaporation**

Disadvantages:
- Poor film uniformity
- Poor step coverage

1) Source material is melted by e-beam directly deposited on wafer
2) Simple and relatively inexpensive
3) Better thickness control
4) Higher film purity
5) Increasing of the E-beam energy yields higher density film with better adhesion to substrate
6) Widely used for lift-off process
7) Multi-layer deposition

<table>
<thead>
<tr>
<th>Sputtering &amp; Evaporation</th>
<th>SPT-3180</th>
<th>P2-01000</th>
<th>Varian 3180 Sputter</th>
<th>Semi-Clean</th>
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<tr>
<td>SPT-AST600</td>
<td>EC-01000</td>
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<tr>
<td>SPT-AST450</td>
<td>EC-01000</td>
<td>AST 450I Evaporator</td>
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</table>
Process modules in NFF

1. Photolithography
2. Cleaning and Wet etching
3. Thin film growth and deposition
4. Implantation
5. Dry Etching
6. Grinding and Polishing
7. Metrology
4. Ion Implantation

• Ions are accelerated and forced to the substrate/film by momentum transfer

- Full wafers are preferred
- Irregular samples have to be bounded on full wafers
- Spices (B, BF$_2$, As, P, H)
- Dosage (1E12~1E16)
- High Temperature Photoresist (Special for implantation $FH$-$6400L$)
- Wafers with no resist on the rim and back side
- No exposed metals
Implantation profile

Two important parameters:
Energy (KeV): Implantation depth
Dosage (cm\(^{-2}\)): Concentration

Gaussian distribution

B in Si
Dose: \(10^{15}\) cm\(^{-2}\)

Implant Mask

\[ \Delta R_p \]

Depth [\(\mu m\)]

Concentration [cm\(^{-3}\)]
Process modules in NFF

1. Photolithography
2. Cleaning and Wet etching
3. Thin film growth and deposition
4. Implantation
5. Dry Etching
6. Grinding and Polishing
7. Metrology
5. Dry Etching

5.1 Non-plasma based

- Typically fluorine-containing gases that readily etch Si
  \[ 2\text{XeF}_2 + Si \rightarrow 2\text{Xe}(g) \uparrow + \text{SiF}_4(g) \uparrow \]
- Highly selective to masking layers (SiO$_2$)
- Highly controllable via temperature and partial pressure of reactants
- Widely used for MEMS fabrication

Equipment: Clean / Semi-clean

XeF$_2$ Isotropic Silicon Etcher (DRY-XeF$_2$)

5.2 Plasma based

- Plasma etching is a process in which a solid film is removed by a chemical reaction with ground-state or excited-state neutral species.
- Types of plasma based etching:
  - Physical sputtering
    - Physical bombardment
  - Plasma etching
    - Plasma assisted chemical reaction
  - Reactive Ion etching (RIE)
    - Chemical Reaction + Ion Bombardment
What is plasma?
Plasma is partially ionized gas containing an equal number of positive and negative charges, as well as some other number of none ionized gas particles. It can be created using electrical fields.

Etching Mechanism
(1) Generation of etching species
(2) Diffusion to surfaces
(3) Adsorption on surface
(4) Reaction & Bombardment
(5) Desorption (Gaseous by-product)
(6) Diffusion into bulk gases & pumped out
ICP Etch for high quality etch

ICP: Inductively Coupled Plasma

ICP: A 13.6 MHz RF power for Coil electrode (plasma source) producing electromagnetic induction, generating high density of ions, to realize high etch rate

RF: a 13.56 MHz RF power magnetic field to create directional electric fields to achieve more anisotropic etch

Advantages:
- Higher plasma density at low pressure
- Better profile
- Lower ion damage
- Faster etching rate
Deep silicon etch (DRIE)

Bosch process:
1. High aspect ratio of silicon etching
2. Separated etching and sidewall passivation steps

Flow rate

SF$_6$

C$_4$F$_8$

Etch

Polymer Deposit

Etch

Mask

F

SF$_x^+$

F

nCF$_x^+$

SF$_x^+$

<table>
<thead>
<tr>
<th>Process code</th>
<th>Location</th>
<th>Equipment</th>
<th>Cleanliness level</th>
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<tr>
<td>DRY-Si-1</td>
<td>P2-01000</td>
<td>DRIE Etcher #1</td>
<td>Clean</td>
</tr>
<tr>
<td>DRY-Si-2</td>
<td>Rm.2223</td>
<td>DRIE Etcher #2</td>
<td>Clean/Semi-Clean</td>
</tr>
<tr>
<td>DRY-Si-2</td>
<td>Rm.2223</td>
<td>DRIE Etcher #3</td>
<td>Non-Standard</td>
</tr>
</tbody>
</table>

Scallops after DRIE etch
Pictures from SPTS
Process modules in NFF

1. Photolithography
2. Cleaning and Wet etching
3. Thin film growth and deposition
4. Implantation
5. Dry Etching
6. Grinding and Polishing
7. Metrology
Grinding

- Silicon Grinder (NanoFactor NVG-200A) is composed of grinding main body and control panel.
- Using a rotating diamond grinding wheel to thin sample thickness with accuracy in the order of micrometers.
- Remove thickness: 20~400µm
- Whole wafer
Polishing

- EcoMet™300 polisher (Buehler Polisher #1, #2) is composed of power head, D-shape bowl and control panel.
- Mechanical polish of sample surface using different size of slurry and different type of polish cloth.
- Slurry size: 15µm, 9µm, 6µm, 3µm, 1µm, and 0.06µm.
- Final surface roughness: ~1nm
CMP (Chemical Mechanical Planarization)

CMP is a process that removes material from the wafer surface by means of synergistic chemical and mechanical actions.

Polish material: SiO₂, Poly-Si
Substrate size: 4” wafer only
Wafer thickness: 400-550µm
Slurry: For Oxide: Cabot SS 25E (PH=10.2-11.2) (Silica <12-25%, KOH<1%, DI water >74-87%
For Poly-Si: P-1000 (PH=9.5-10.5) (Silica <5%, DI Water>92%)
Process modules in NFF

1. Photolithography
2. Cleaning and Wet etching
3. Thin film growth and deposition
4. Implantation
5. Dry Etching
6. Grinding and Polishing
7. Metrology
Metrology

Microscope

Surface profiler

4-point probe for sheet resistance

Ellipsometer

Atomic Force Microscope (AFM)

Scanning Electron Microscope (SEM)
Aim of Process Flows

Functions:
- Help you to plan ahead
- Track down wafer movement
- Reduce uncertainty
- keep the unqualified away from NFF

Aim:
- Control Contamination
## Process Flow of XXX XXX XXX

### Project: Cross-section

**MASK 0**
- **Wafer Cleanliness:** Clean
- **Substrate:** Si Substrate
- **Silicon oxide:**
  - **Clean:**
  - **Silicon oxide:**
  - **Si Substrate:**

<table>
<thead>
<tr>
<th>Step No.</th>
<th>Equipment</th>
<th>Location</th>
<th>Cleanliness</th>
<th>Process</th>
<th>Requirements</th>
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</thead>
<tbody>
<tr>
<td>0.1</td>
<td>A3: Sulfuric Cleaning</td>
<td>P201000</td>
<td>Clean</td>
<td>Initial Clean</td>
<td>H2SO4 + H2O2, 10mins, 120C</td>
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<tr>
<td>0.2</td>
<td>A2: HF:H2O (1:50)</td>
<td>P201000</td>
<td>Clean</td>
<td>HF dip</td>
<td>1 min</td>
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<tr>
<td>0.3</td>
<td>Spin Dryer-A</td>
<td>P201000</td>
<td>Clean</td>
<td>Dry the wafer automatically</td>
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<tr>
<td>0.4</td>
<td>Diff. Furnace-D2 Dry/Wet Oxidation</td>
<td>P201000</td>
<td>Clean</td>
<td>Sacrificial Oxide Growth</td>
<td>200A</td>
</tr>
</tbody>
</table>

**MASK 1**
- **Wafer Cleanliness:** Clean/Semi-Clean
- **Substrate:** Si Substrate
- **Al/Si-1%:**
  - **Silicon oxide:**
  - **Si Substrate:**

<table>
<thead>
<tr>
<th>Step No.</th>
<th>Equipment</th>
<th>Location</th>
<th>Cleanliness</th>
<th>Process</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>B1: Sulfuric Cleaning</td>
<td>P201000</td>
<td>Semi-Clean</td>
<td>Standard Cleaning</td>
<td>10mins, 120C</td>
</tr>
<tr>
<td>1.2</td>
<td>Spin Dryer-B</td>
<td>P201000</td>
<td>Semi-Clean</td>
<td>Dry the wafer automatically</td>
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<tr>
<td>1.3</td>
<td>SVG Coater Track</td>
<td>P200100</td>
<td>Clean/Semi-Clean</td>
<td>HMDS, PR coating, soft bake</td>
<td>AZ 504, 1.2µm, soft bake: 110C 1min</td>
</tr>
<tr>
<td>1.4</td>
<td>Karl Suss MA6 #2</td>
<td>P200100</td>
<td>Clean/Semi-Clean</td>
<td>Define oxide pad</td>
<td>5s</td>
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<tr>
<td>1.5</td>
<td>SVG Developer Track</td>
<td>P200100</td>
<td>Clean/Semi-Clean</td>
<td>Develop, Hard bake</td>
<td>FHD-5, 1min; hard bake: 120C, 1min</td>
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<tr>
<td>1.6</td>
<td>C3: BOE</td>
<td>P201000</td>
<td>Clean</td>
<td>Oxide Etch</td>
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<tr>
<td>1.7</td>
<td>E4: Resist Strip</td>
<td>P201000</td>
<td>Clean/Semi-Clean</td>
<td>Sulfuric resist strip</td>
<td>H2SO4 + H2O2,120C, 10mins</td>
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<td>Spin dry</td>
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<td>Varian 3180 Sputter</td>
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<td>Aluminum Sputtering</td>
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</table>

**MASK 2**
- **Wafer Cleanliness:** Semi-Clean
- **Substrate:** Si Substrate
- **Gold:**
  - **Al:**
  - **Silicon oxide:**
  - **Si Substrate:**

<table>
<thead>
<tr>
<th>Step No.</th>
<th>Equipment</th>
<th>Location</th>
<th>Cleanliness</th>
<th>Process</th>
<th>Requirements</th>
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<td>P200100</td>
<td>Clean/Semi-Clean</td>
<td>HMDS, PR coating, soft bake</td>
<td>AZ 504, 1.2µm, soft bake: 110C 1min</td>
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<tr>
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<td>Karl Suss MA6 #2</td>
<td>P200100</td>
<td>Clean/Semi-Clean</td>
<td>Al Patterning</td>
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<td>P200100</td>
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<td>Develop and hard bake</td>
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<td>Semi-Clean</td>
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<td>Y1: MS2001</td>
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<td>Process</td>
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<td>W2: FHD-5</td>
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<td>Develop &amp; Rinsing</td>
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<td>Spin Dryer-W</td>
<td>P200100</td>
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<td>Spin dry</td>
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<td>Non-Standard</td>
<td>2.8</td>
<td>Shellab (120C)</td>
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<td>Non-standard</td>
<td>Hard bake</td>
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<td>W1: MS2001 Resist Strip</td>
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</tbody>
</table>
## Mistake 1 - Oversimplification

### Cross-Section

**MASK 0**

- **Thermal oxide**
- **Si Substrate**

### Table: Wafer Cleanliness

<table>
<thead>
<tr>
<th>Step No.</th>
<th>Equipment</th>
<th>Location</th>
<th>Cleanliness</th>
<th>Process</th>
<th>Requirements</th>
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</thead>
<tbody>
<tr>
<td>0.1</td>
<td>A3: Sulfuric Cleaning</td>
<td>P201000</td>
<td>Clean</td>
<td>Initial Clean</td>
<td>H2SO4 + H2O2, 10mins, 120°C</td>
</tr>
<tr>
<td>0.2</td>
<td>A2: HF:H2O (1:50)</td>
<td>P201000</td>
<td>Clean</td>
<td>HF dip</td>
<td>1 min</td>
</tr>
<tr>
<td>0.3</td>
<td>Spin Dryer-A</td>
<td>P201000</td>
<td>Clean</td>
<td>Dry the wafer automatically</td>
<td></td>
</tr>
<tr>
<td>0.4</td>
<td>Diff. Furnace-D2 Dry/Wet Oxidation</td>
<td>P201000</td>
<td>Clean</td>
<td>Sacrificial Oxide Growth</td>
<td>200A</td>
</tr>
</tbody>
</table>
## Mistake 2 – Improper process steps

### Nitride deposition

#### Cross-Section

<table>
<thead>
<tr>
<th>Wafer Cleanliness</th>
<th>Step No.</th>
<th>Equipment</th>
<th>Location</th>
<th>Cleanliness</th>
<th>Process</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clean</td>
<td>0.1</td>
<td>A3: Sulfuric Cleaning</td>
<td>P201000</td>
<td>Clean</td>
<td>Initial Clean</td>
<td>H2SO4 + H2O2, 10mins, 120C</td>
</tr>
<tr>
<td>Clean</td>
<td>0.2</td>
<td>A2: HF:H2O (1:50)</td>
<td>P201000</td>
<td>Clean</td>
<td>HF dip</td>
<td>1 min</td>
</tr>
<tr>
<td>Clean</td>
<td>0.3</td>
<td>Spin Dryer-A</td>
<td>P201000</td>
<td>Clean</td>
<td>Dry the wafer automatically</td>
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<td>LPCVD-B2 Nitride/Low-Stress Nitride</td>
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<td>Clean</td>
<td>Nitride deposition</td>
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</table>
### Mistake 3 – Incompatible equipment

#### Wafer Cleanliness

<table>
<thead>
<tr>
<th>Step No.</th>
<th>Equipment</th>
<th>Location</th>
<th>Cleanliness</th>
<th>Process</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>B1: Sulfuric Cleaning</td>
<td>P201000</td>
<td>Clean</td>
<td>Standard Cleaning</td>
<td>10mins, 120C</td>
</tr>
<tr>
<td>1.2</td>
<td>Spin Dryer-B</td>
<td>P201000</td>
<td>Clean</td>
<td>Dry the wafer automatically</td>
<td></td>
</tr>
<tr>
<td>1.3</td>
<td>SVG Coater Track</td>
<td>P200100</td>
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<td>P200100</td>
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<td>1.5</td>
<td>SVG Developer Track</td>
<td>P200100</td>
<td>Clean/Semi-Clean</td>
<td>Develop and hard bake</td>
<td>PHD-5, 1min; 120C, 1min</td>
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<td>1.6</td>
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<td>P201000</td>
<td>Clean</td>
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<td>Spin Dry</td>
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<td>1.9</td>
<td>Varian 3180 Sputter</td>
<td>P201000</td>
<td>Semi-Clean</td>
<td>Aluminum Sputtering</td>
<td>4000A</td>
</tr>
</tbody>
</table>

#### Si Substrate

- **Al (3180 sputtered)**
- **Silicon oxide**
- **Si Substrate**

#### How to modify?

1. Use another aligner Karl Suss MA6#2 (Clean/Semi-Clean) to do exposure. The wafer status will be “Clean” before Al sputtering
2. Use Wetsation D to do oxide etch (Semi-Clean)
### Mistake 3 - Incompatible equipment

**Wafer Cleanliness**
- **Clean**
- **Semi-Clean**

**Step No.** | **Equipment** | **Location** | **Cleanliness** | **Process** | **Requirements**
--- | --- | --- | --- | --- | ---
1.1 | B1: Sulfuric Cleaning | P201000 | Clean | Standard Cleaning | 10mins, 120C
1.1 | AB-M Aligner #2 | P201000 | Semi-Clean/Non-Standard | Define Oxide Pad | 6s
1.2 | Spin Dryer-B | P201000 | Clean | Dry the wafer automatically | 
1.3 | SVG Coater Track | P200100 | Clean/Semi-Clean | HMDS, PR Coating, Soft bake | AZ 504, 1.2μm, soft bake: 110C 1min
1.4 | Karl Suss MA6#2 | P200100 | Clean/Semi-Clean | Define Oxide Pad | 6s
1.5 | SVG Developer Track | P200100 | Clean/Semi-Clean | Develop and hard bake | FHD-5,1min; 120C, 1min
1.6 | C3: BOE | P201000 | Clean | Oxide etch | 
1.7 | E4: Resist Strip | P201000 | Clean/Semi-Clean | Resist Stripping (wet) | 10min, 120C
1.8 | Spin Dryer-E | P201000 | Clean/Semi-Clean | Spin Dry | 
1.9 | Varian 3180 Sputter | P201000 | Semi-Clean | Aluminum Sputtering | 4000A

**Note:**
- Silicon oxide
- **Si Substrate**
## Mistake 4 – Double side coating

<table>
<thead>
<tr>
<th>Mask 1</th>
<th>Wafer Cleanliness</th>
<th>Step No.</th>
<th>Equipment</th>
<th>Location</th>
<th>Cleanliness</th>
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Wafer chuck for PR coating

4” Coating Chuck

4” Double coating chuck
### Mistake 5 – Wrong PR Stripping

- **Once there is metal on your sample, it can not be put into E4: Resist Strip (Sulfuric Acid) for PR strip!!!**
- **Otherwise, the Bath will be contaminated.**

After Metal Sputtering, there are two ways to do PR stripping:

1. MS2001
2. O2 Asher
3. Sulfuric Acid **X**
Other Mistakes

- Mistake 6 -- Misuse of Decontamination
- Mistake 7 -- Wafer Edge Coating
- Mistake 8 -- Missing backside rinsing prior to implantation
- Mistake 9 -- Improper etching mask for dry or wet etch
- Mistake 10 -- Improper process parameters beyond the limitation of equipment
Chemicals and Wetstations

- Don’t bring your own chemicals or materials into NFF unless you have approval.
- Don’t take any chemicals or materials away. That is theft.
- Don’t leave chemical bottles on the floor.
- Never put into “Clean” baths wafers that have undergone metallization.
- Don’t leave anything, especially incompatible materials, on the top of wet-stations.
- Disposal of HF and BOE must be done by trained persons.
- Don’t be so irresponsible as to leave down the tools you have used and go away.
- Don’t mix up the gloves, cassettes and tools of one station with those of others. You should look at the labels!
- Clean all the tools and containers you have used and place them back to where they are.
- No ORGANIC Solvent at wetstations in Class 1000.
- No acid and base in Yellow Room.
Operation

- Store wafers of different wafer status in separate boxes
- Always inspect your wafers after a resist strip to ensure cleanliness
- Don’t put Non-Standard materials, especially gold into Semi-Clean and Clean baths
- Don’t put liftoff samples in any processing baths
- Always keep your samples in your own containers or cassette boxes in case they contaminate others or be contaminated.

- Always be careful with photoresist which is very contaminating.
- Arrange Non-Standard steps as close to the end of process flow as possible.
- After cleaning, wafers must go straight to furnaces without being touched by any objects.
Process Flows

- Plan before work. If you fail to plan you are planning to fail
- Follow the process flow format
- Write what you do and do what you write.
- Once your process becomes different from what you have planed, submit us a new flow

- Never copy others’ process flow
- Never let others copy your process flow
- Do let us know, if you find your processes departing from our scheme.
- Proofread before submitting them
Personal

❖ Don’t shortcut any policy and rules
❖ Keep yourself abreast of information about rules and regulations, as it is dynamic and subject to change.
❖ Report to us any mistakes you or others have made. Don’t hide it!
❖ Be aware of contamination that you may cause and others cause

❖ Remember, this is a shared lab. Everyone must follow lab policy to keep it clean
❖ Use your judgment. Avoid contamination of wafers or equipment
❖ Don’t stay in the laboratory if not necessary. NFF is not a meeting place!
❖ Follow the buddy system after office hour
Collection of research publications

- **Acknowledge** NFF using "*We acknowledge Nanosystem Fabrication Facility (NFF) of HKUST for the device / system fabrication.*" in your future publications involving work conducted in NFF. (http://www.nff.ust.hk/en/about-nff/publication.html)

- Upload new publications through our website

![Publication list](image)

Submission

Publications will be shown on NFF news letter and NFF entrance displays
Q and A